MSG2136

600V 3-Phase Half-Bridge Gate Driver

Features

- Floating high side up to +600V
- Gate drive supply ranging from 10V to 20V
- 3 Independent half-bridge drivers
- Under-voltage lockout protection
- Built-in cross-conduction prevention
- Compatible with 3.3/5V logic
- 6 outputs out of phase with respective inputs
- Over current protection by shutdown
- Enable input controls all 3 phases
- FAULT indicators for OCP or OCP conditions
- Programmable delay for automatic fault clear
- Lead-free (ROHS compliant)

Product Summary

V_{OFFSET}	600V
I_{O+}/I_{O-}	190mA/360mA
V_{OUT}	10V-20V
$T_{on/off}$	440ns/400ns
Delay matching	50ns

Descriptions

MSG2136 is 3-phase half bridge gate driver and each phase is capable of driving two IGBTs or N-channel MOSFETs. MSG2136 applies to bootstrap architecture with an external bootstrap diode for each phase. The UVLO prevents abnormal behaviors once VCC or VBS drops lower than the specific threshold voltage. The cross-conduction prevention protects the power switches from simultaneous turn-on. Enable input can terminate all 6 outputs simultaneously. A current trip protection derived from an external sense resistor can terminate all outputs once over current occurs. An open-drain FAULT signal indicate over-current or under-voltage has occurred. Over-current conditions are automatically cleared after a delay programmed by an RC network connected to the RCIN input.

Ordering Information

Part No.	Package Type	Packing Form
MSG2136	SOP-28	Tape & Reel

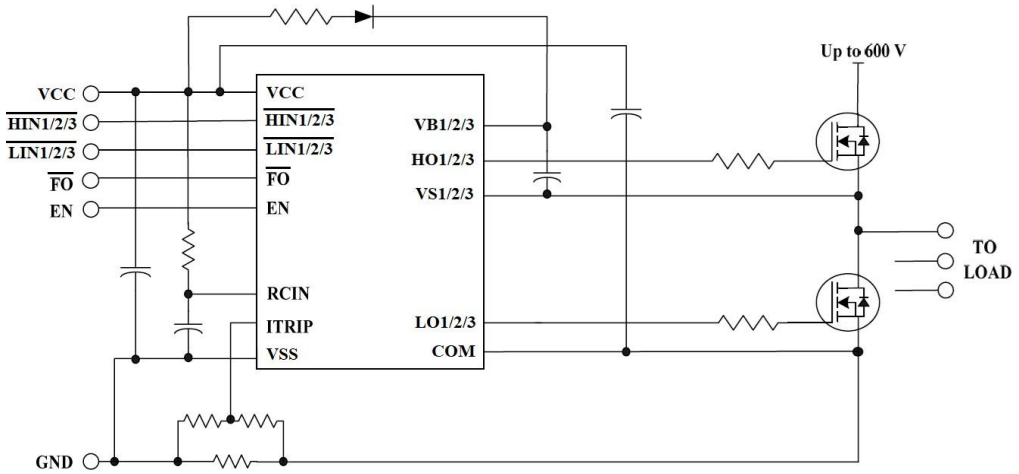


Figure 1. Typical configuration

Pin Definitions and Assignments

Figure 2. Pin assignment (28-Lead SOIC)

Pin #	Symbol	Description
1	VCC	Low side & logic power supply
2/3/4	$\overline{\text{HIN1/2/3}}$	Logic inputs for high side gate driver outputs (HO1/2/3), out of phase
5/6/7	$\overline{\text{LIN1/2/3}}$	Logic inputs for low side gate driver outputs (LO1/2/3), out of phase
8	$\overline{\text{FAULT}}$	Open-drain negative logic output indicating ITRIP OCP or low side UVLO
9	ITRIP	Analog input for over-current shutdown and activate FAULT & RCIN low
10	EN	Logic input to enable I/O functions. No effect on FAULT.
11	RCIN	High side gate driver output
12	VSS	Logic ground
13	COM	Low side power supply return
14/15/16	LO1/2/3	Low side gate driver outputs
18/22/26	VS1/2/3	High side floating power supply return
19/23/27	HO1/2/3	High side gate driver outputs
20/24/28	VB1/2/3	High side floating power supply
17/21/25	NC	No connection

Functional Block Diagram

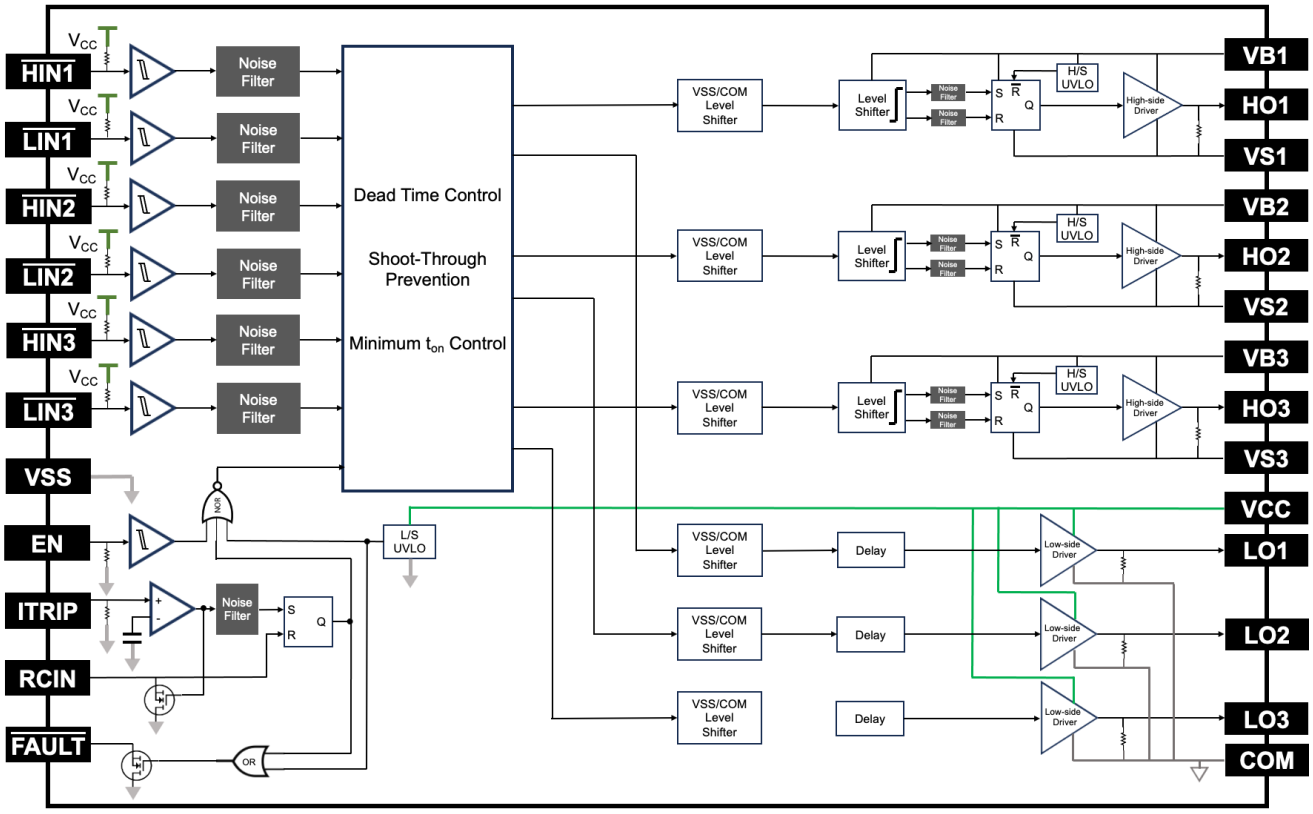


Figure 3. Functional block diagram

Absolute Maximum Ratings

All voltages are absolute voltage referenced to V_{COM} unless otherwise specified. (T_A=+ 25 °C)

Symbol	Parameter	Min	Max	Unit
V_B	High side floating supply voltage	-0.3	600	V
V_S	High side floating supply offset voltage	V_B-20	V_B+0.3	
V_{HO}	High side floating output voltage	V_S-0.3	V_B+0.3	
V_{CC}	Low side and logic fixed supply voltage	-0.3	20	
V_{LO}	Low side output voltage	-0.3	V_{CC}+0.3	
V_{IN}	Input voltage ($\overline{HIN1/2/3}$, $\overline{LIN1/2/3}$, EN, ITRIP)	-0.3	V_{CC}+0.3	
V_{RCIN}	RC network input voltage	-0.3	V_{CC}+0.3	
V_{FAULT}	$\overline{FAULT}$ output voltage	-0.3	V_{CC}+0.3	
dV/dt	Allowable common mode transient	-	50	V/ns
P_D	Package power dissipation @ $T_A \leq$ + 25 °C (1)	-	1.6	W
Rth_{JA}	Thermal resistance, junction to ambient (2)	-	78	°C/W
T_J	Junction temperature	-	150	°C
T_S	Storage temperature	-55	150	

(1) Total power dissipation depends on package and mounting conditions, here is based on 28-lead SOIC package.
(2) Thermal resistance depends on package and mounting conditions, here is based on 28-lead SOIC package.

Recommended Operating Conditions

All voltages are absolute voltage referenced to V_{COM} unless otherwise specified. (T_A=+ 25 °C)

Symbol	Parameter	Min	Max	Unit
V_B	High side floating supply voltage (V_B1/2/3)	V_S+12	V_S+18	V
V_S	High side floating supply offset voltage (V_S1/2/3)	-6	450	
V_{HO}	High side floating output voltage (HO1/2/3)	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage (V_{CC})	12	18	
V_{LO}	Low side output voltage (LO1/2/3)	0	V_{CC}	
V_{IN}	Input voltage ($\overline{HIN1/2/3}$, $\overline{LIN1/2/3}$, EN, ITRIP)	0	5	
V_{RCIN}	RC network input voltage	0	V_{CC}	
V_{FAULT}	$\overline{FAULT}$ output voltage	0	V_{CC}	
DT	$\overline{HIN}$ & $\overline{LIN}$ dead time (depends on MCU control)	1	-	µs
T_A	Ambient temperature	-40	125	°C

Static Electrical Characteristics

V_{CC}=V_{BS}= 15V unless otherwise specified (T_A=+ 25 °C)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{IH}	Logic " 1 " input voltage	-	2.3	-	V	$\overline{HIN1/2/3}$, $\overline{LIN1/2/3}$, EN Vcc=10V~20V
V_{IL}	Logic " 0 " input voltage	-	1.3	-		
V_{I_HYS}	V_{IH} V_{IL} input hysteresis	-	1.0	-		
$V_{ITRIP,TH+}$	ITRIP positive going threshold	-	0.48	-		
$V_{ITRIP,HYS}$	ITRIP input hysteresis	-	0.06	-		
$V_{RCIN,TH+}$	RCIN positive going threshold	-	8.0	-		
$V_{RCIN,HYS}$	RCIN input hysteresis	-	3.0	-		
V_{CCUV+} V_{BSUV+}	V_{CC}/V_{BS} supply under voltage positive going threshold	-	9.0	-		
V_{CCUV-} V_{BSUV-}	V_{CC}/V_{BS} supply under voltage negative going threshold	-	8.0	-		
V_{CCUVH} V_{BSUVH}	V_{CC} and V_{BS} supply under voltage lockout hysteresis	-	1.0	-		
I_{LK}	Offset supply leakage current	-	-	50	μA	V_B=V_S=600V
I_{QCC1}	Quiescent V_{CC} supply current	-	510	-		LO=Low
I_{QCC2}	Quiescent V_{CC} supply current	-	1220	-		LO=High
I_{QBS1}	Quiescent V_{BS} supply current	-	80	-		HO=Low
I_{QBS2}	Quiescent V_{BS} supply current	-	400	-		HO=High
I_{IN+}	Logic " 1 " input bias current	-	85	220		$\overline{HIN}$=$\overline{LIN}$=0V
I_{IN-}	Logic " 0 " input bias current	-	0	-		$\overline{HIN}$=$\overline{LIN}$=15V
I_{ITRIP+}	Logic " 1 " ITRIP input bias current	-	55	-		ITRIP=5V
I_{ITRIP-}	Logic " 0 " ITRIP input bias current	-	0	-		ITRIP=0V
I_{EN+}	Logic " 1 " EN input bias current	-	55	-		EN=5V
I_{EN-}	Logic " 0 " EN input bias current	-	0	-		EN=0V
I_{O+}	Output source current	-	190	-	mA	VO=0V, PW≤10μs
I_{O-}	Output sink current	-	360	-		VO=15V, PW≤10μs
R_{ON_RCIN}	RCIN low on-resistance	-	50	80	Ω	
R_{ON_FAULT}	$\overline{FAULT}$ low on-resistance	-	50	80		

Dynamic Electrical Characteristics

V_{CC}=V_{BS}= 15V and C_L=1nF unless otherwise specified (T_A=+ 25 °C)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{on}	HIN/LIN turn-on propagation delay	V_S=0V	-	440	-	ns
t_{off}	HIN/LIN turn-off propagation delay	V_S=0V	-	400	-	
t_r	HO/LO turn on rise time	V_S=0V	-	115	-	
t_f	HO/LO turn off fall time	V_S=0V	-	55	-	
t_{ITRIP}	ITRIP to output shutdown propagation delay	V_{TRIP}=5V	-	250	-	
$t_{b,ITRIP}$	ITRIP blanking time		-	150	-	
t_{FAULT}	ITRIP to $\overline{FAULT}$ propagation delay		-	170	-	
t_{EN}	EN low to output shutdown propagation delay		-	250	-	
t_{FLT}	Input effective filter time ($\overline{HIN1/2/3}$, $\overline{LIN1/2/3}$)		-	250	-	
t_{FLTCLR}	$\overline{FAULT}$ clear time (time constant=2E-3)	V_{TRIP}=0V	-	1.7	-	ms
DT	Deadtime, LS turn-off to HS turn-on & HS turn-off to LS turn-on		-	350	-	ns
MT	Delay matching, HS & LS turn-on/off		-	50	-	

Timing Diagrams

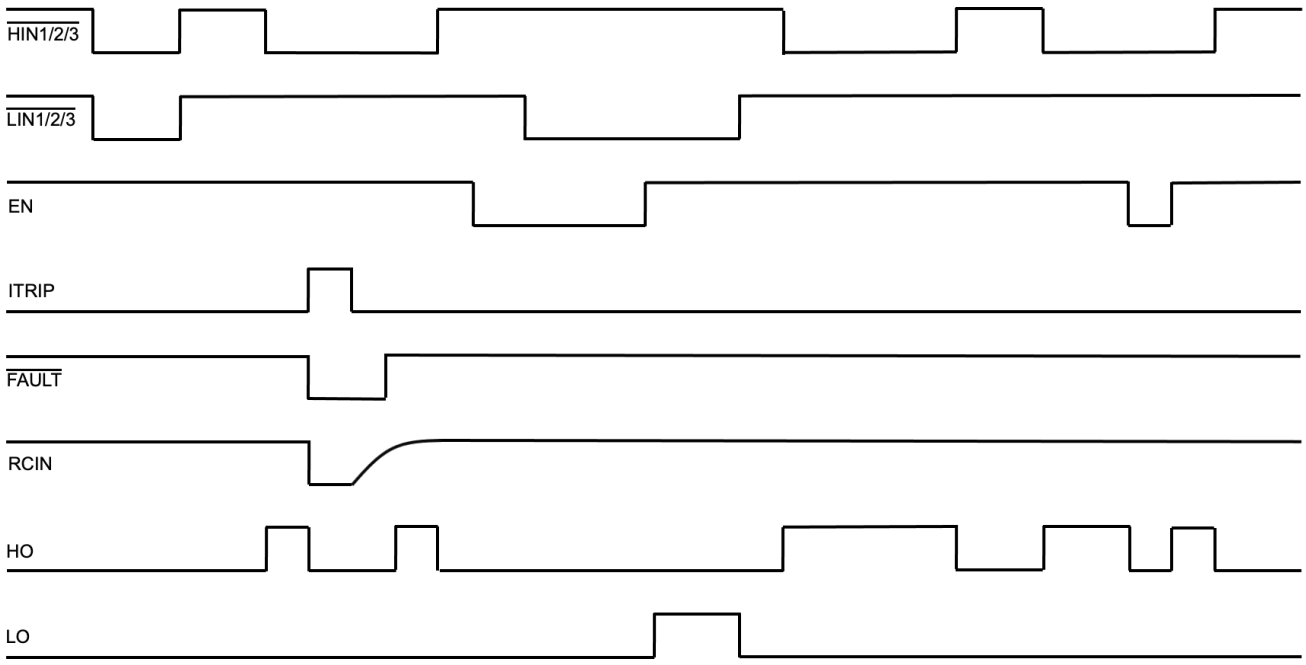


Figure 4. Input/output timing diagram

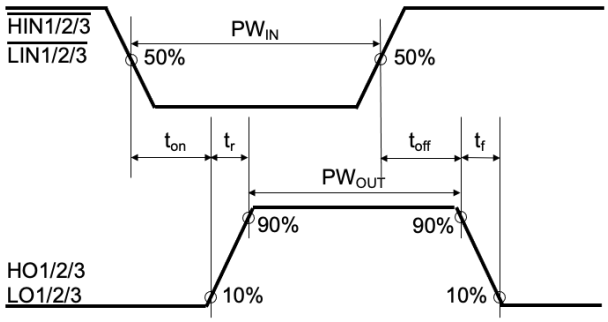


Figure 5. Switching time waveforms

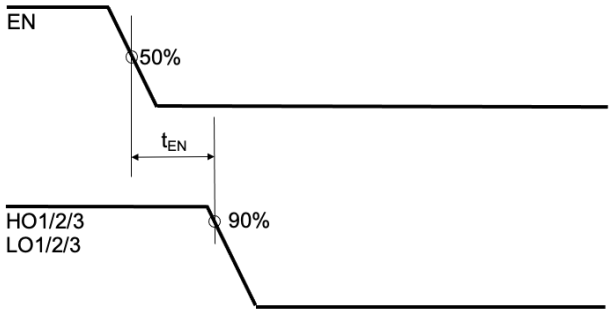


Figure 6. Output enable (EN) timing waveform

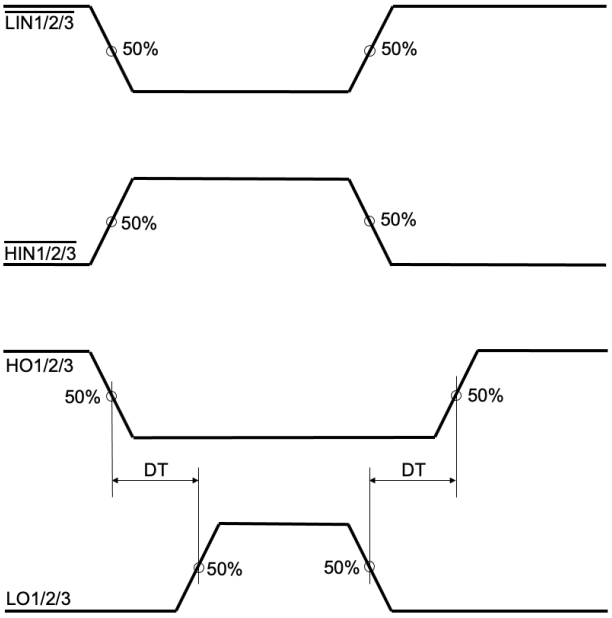


Figure 7. Deadtime timing waveforms

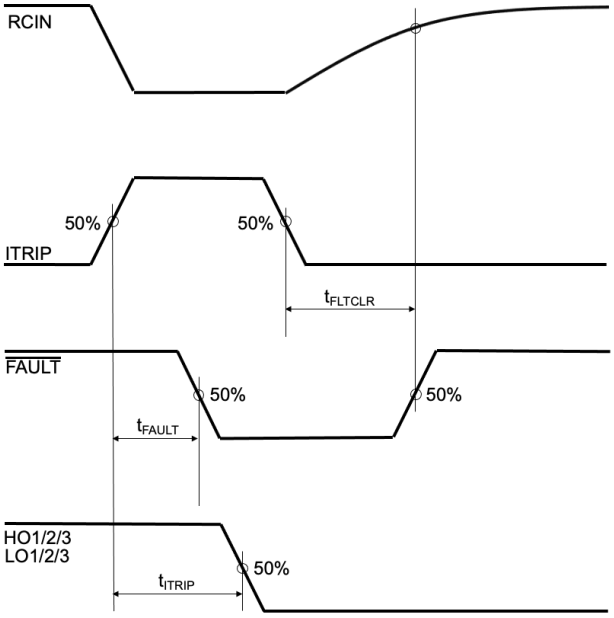
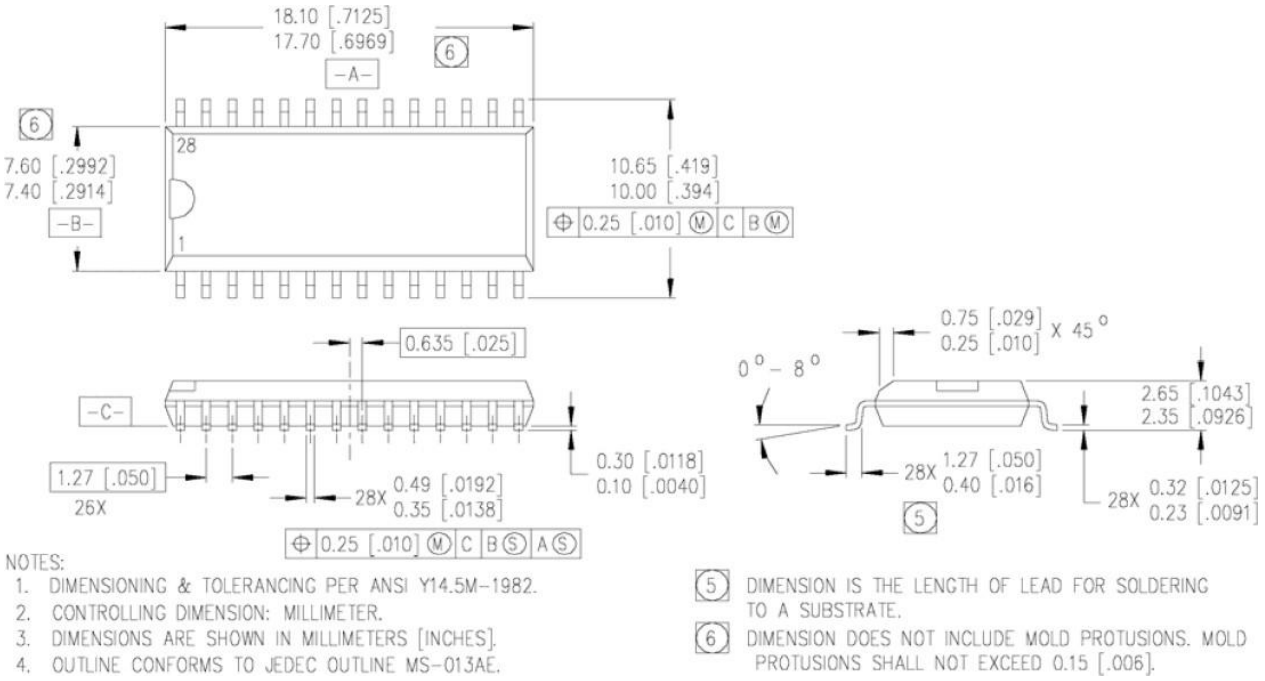


Figure 8. ITRIP/RCIN timing waveforms

Package Information

SOP-28



NOTES:
1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-013AE.

(5) DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

(6) DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].