MSG2103

600V Half-Bridge Gate Driver

Features

- Floating high side up to +600V
- Gate drive supply ranging from 10V to 20V
- Under-voltage lockout protection
- Built-in cross-conduction prevention
- Compatible with 3.3V/5V logic
- Outputs in phase with inputs
- Lead-Free (ROHS Compliant)

Product Summary

V_{OFFSET}	600V
I_{O+}/I_{O-}	220mA/380mA
V_{OUT}	10V-20V
$T_{on/off}$	450ns/420ns
Delay matching	50ns

Description

MSG2103 is half-bridge pre-driver IC and capable of driving a pair of power devices (IGBT/N-MOSFET). MSG2103 applies to typical bootstrap architecture with an external bootstrap diode for each phase. The UVLO prevents abnormal behaviors once VCC or VBS drops lower than the specific threshold voltage. The cross-conduction prevention protects the power devices from simultaneous turn-on due to noise or flicker of control logic.

Ordering Information

Part No.	Package Type	Packing Form
MSG2103	SOP-8	Tape & Reel

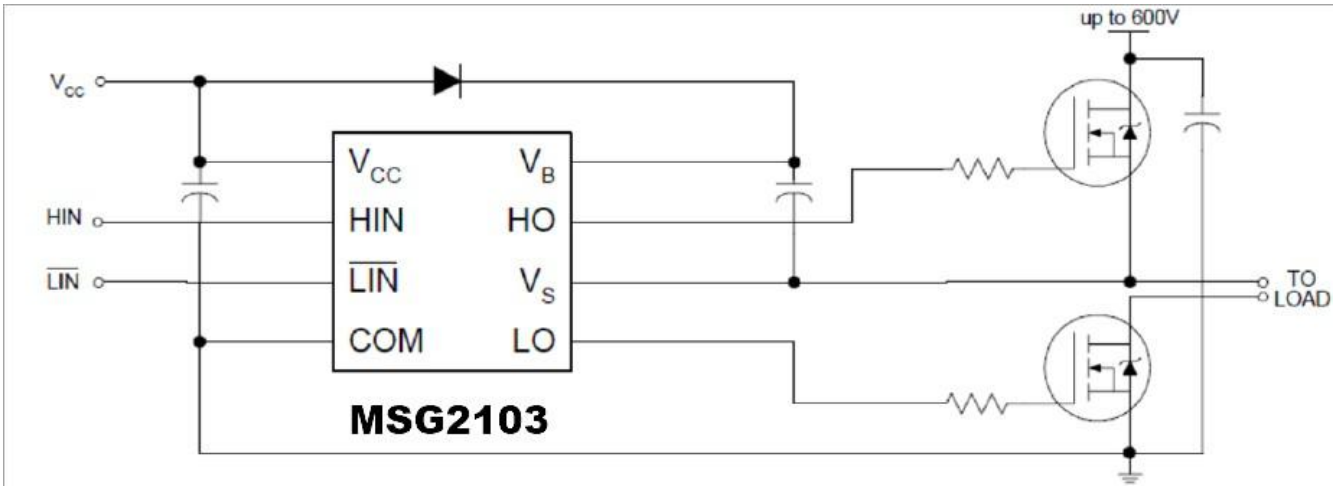


Figure 1. Typical configuration

Pin Assignments & Definition

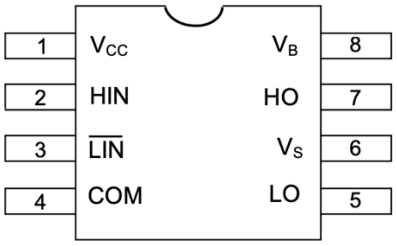


Figure 2. Pin assignment (8-Lead SOIC)

Pin #	Symbol	Description
1	V_{CC}	Low side power supply
2	HIN	Logic input for high side gate driver output (HO), in phase
3	$\overline{LIN}$	Logic input for low side gate driver output (LO), out of phase
4	COM	Low side return
5	LO	Low side gate driver output
6	V_S	High side floating supply return
7	HO	High side gate driver output
8	V_B	High side power supply

Functional Block Diagram

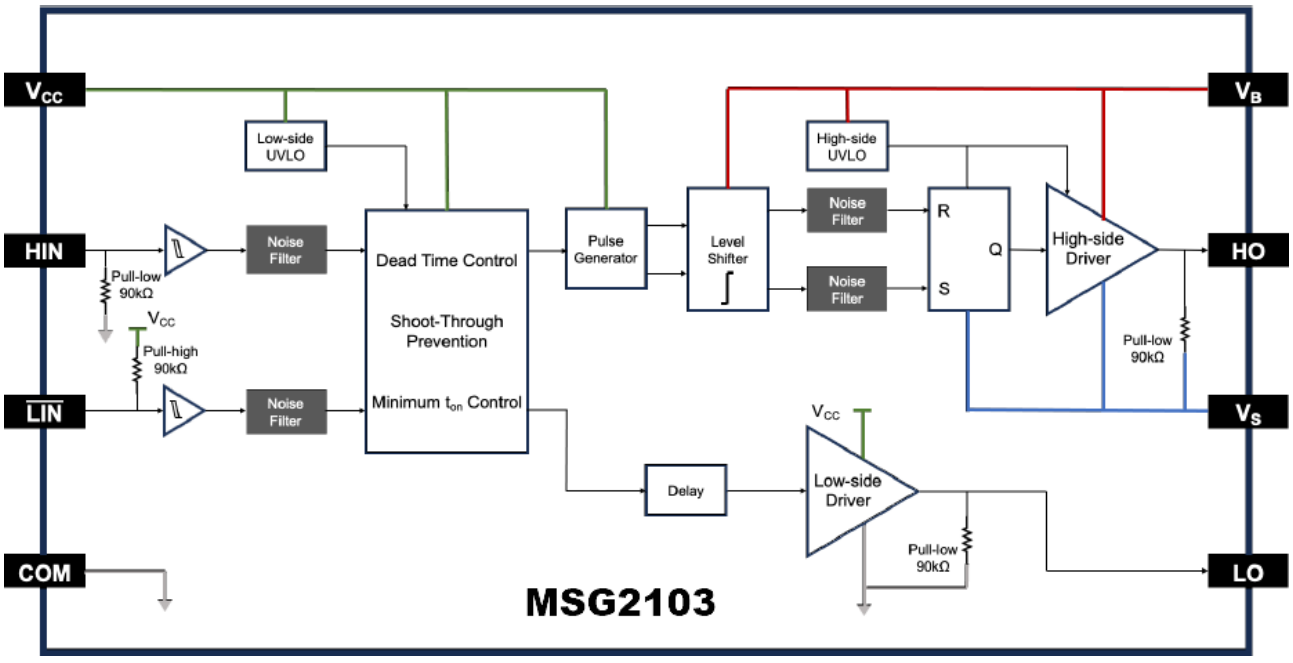


Figure 3. Functional block diagram

Absolute Maximum Ratings

All voltages are absolute voltage referenced to V_{COM} unless otherwise specified. (T_A=25℃)

Symbol	Parameter	Min	Max	Unit
V_B	High side floating supply voltage	-0.3	600	V
V_S	High side floating supply offset voltage	V_B-20	V_B+0.3	
V_{HO}	High side floating output voltage	V_S-0.3	V_B+0.3	
V_{CC}	Low side and logic fixed supply voltage	-0.3	20	
V_{LO}	Low side output voltage	-0.3	V_{CC}+0.3	
V_{IN}	Logic input voltage (HIN & $\overline{LIN}$)	-0.3	V_{CC}+0.3	
dV_S/dt	Allowable offset supply voltage transient	-	50	V/ns
P	Package power dissipation @ $T_A \leq +25\,^oC$ (1)	-	0.625	W
Rth_{JA}	Thermal resistance, junction to ambient (2)	-	200	$^oC/W$
T_J	Junction temperature	-	150	^oC
T_S	Storage temperature	-55	150	

(1) Total power dissipation depends on package and mounting conditions, here is based on 8 leads SOIC package.
(2) Thermal resistance depends on package and mounting conditions, here is based on 8 leads SOIC package.

Recommended Operating Conditions

All voltages are absolute voltage referenced to V_{COM} unless otherwise specified. (T_A=25℃)

Symbol	Parameter	Min	Max	Unit
V_B	High side floating supply absolute voltage	V_S-12	V_S+18	V
V_S	High side floating supply offset voltage	-6	450	
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side and logic fixed supply voltage	12	18	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	Logic and analog input voltage	0	5	
DT	HIN & $\overline{LIN}$ dead time (depends on MCU control)	1	-	µs
T_A	Ambient temperature	-40	125	^oC

Static Electrical Characteristics

V_{CC}=V_{BS}= 15V unless otherwise specified (T_A=25℃)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{IH}	Logic " 1 " input voltage	-	2.5	-	V	V_{CC}=10V~20V
V_{IL}	Logic " 0 " input voltage	-	2.2	-		V_{CC}=10V~20V
V_{I_HYS}	V_{IH} V_{IL} input hysteresis	-	0.3	-		V_{CC}=10V~20V
V_{CCUV+} V_{BSUV+}	V_{CC}/V_{BS} supply under voltage positive going threshold	-	9.0	-		
V_{CCUV-} V_{BSUV-}	V_{CC}/V_{BS} supply under voltage negative going threshold	-	8.0	-		
V_{CCUVH} V_{BSUVH}	V_{CC} and V_{BS} supply under voltage lockout hysteresis	-	1.0	-		
I_{LK}	Offset supply leakage current	-	-	50	μA	V_B=V_S=600V
I_{QCC1}	Quiescent V_{CC} supply current	-	125	-		LO=Low
I_{QCC2}	Quiescent V_{CC} supply current	-	275	-		LO=High
I_{QBS1}	Quiescent V_{BS} supply current	-	90	-		HO=Low
I_{QBS2}	Quiescent V_{BS} supply current	-	240	-		HO=High
I_{IN+}	Logic " 1 " input bias current	-	60	220		HIN=5V, $\overline{LIN}$=0V
I_{IN-}	Logic " 0 " input bias current	-	0	-		HIN=0V, $\overline{LIN}$=5V
I_{O+}	Output source current	-	220	-	mA	VO=0V, PW≤10μs
I_{O-}	Output sink current	-	380	-		VO=15V, PW≤10μs

Dynamic Electrical Characteristics

V_{CC}=V_{BS}= 15V, C_L=1nF unless otherwise specified (T_A=25℃)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{on}	HIN/LIN turn-on propagation delay	V_S=0V	-	450	-	ns
t_{off}	HIN/LIN turn-off propagation delay	V_S=0V	-	420	-	
t_r	HO/LO turn on rise time	V_S=0V	-	82	-	
t_f	HO/LO turn off fall time	V_S=0V	-	46	-	
DT	Deadtime, LS turn-off to HS turn-on & HS turn-off to LS turn-on		-	350	-	
MT	Delay matching, HS & LS turn-on/off		-	50	-	

Timing Diagrams

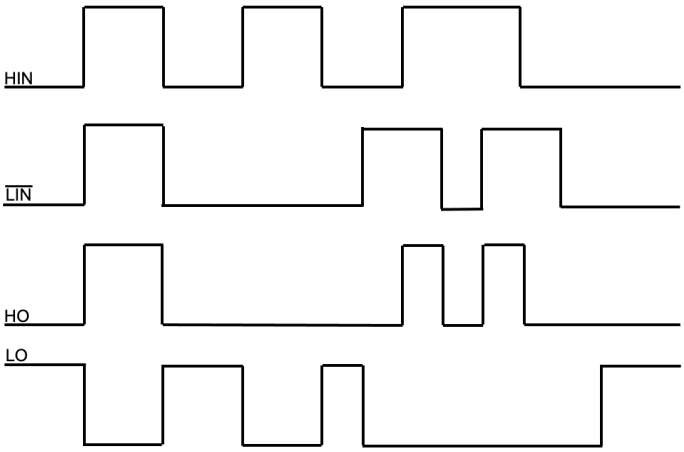


Figure 4. Input/output timing diagram

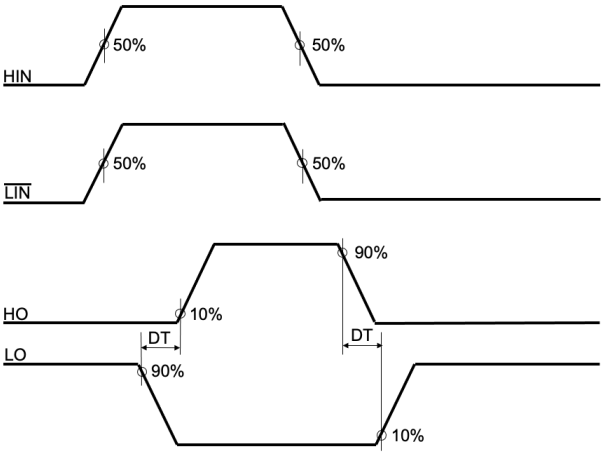
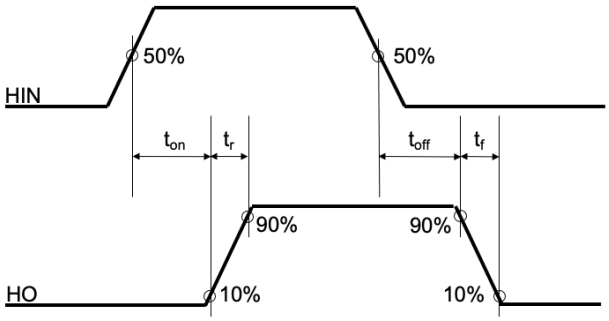


Figure 5. Deadtime timing waveforms



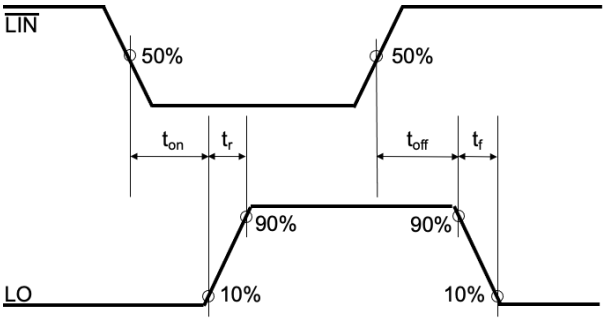
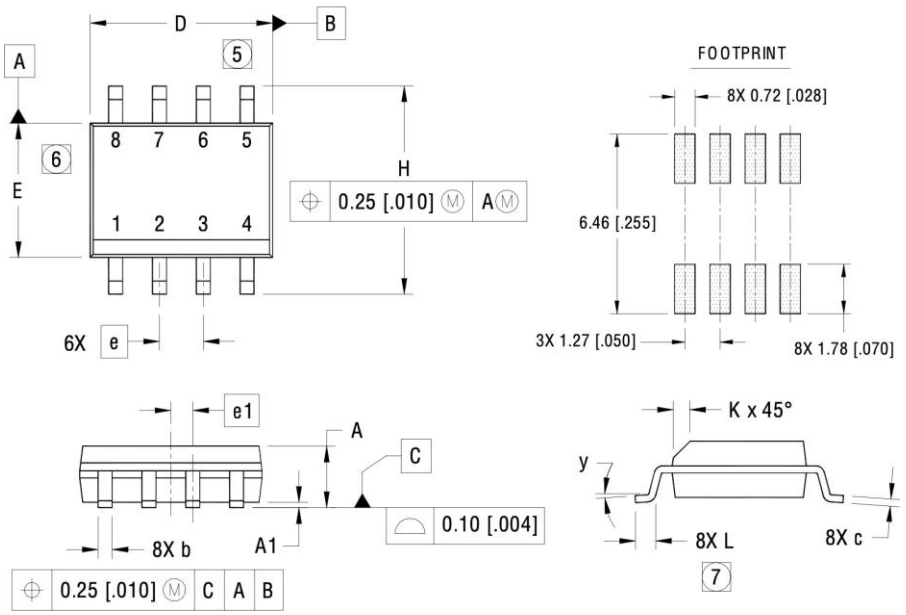


Figure 6. Switching time waveforms

Package Information

SOP-8



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTE

1. Dimensions and tolerances abide by ASME Y14.5M-1994.
2. Controlling dimension: mm.
3. Dimensions are shown in mm [inch].
4. Outline conforms to JEDEC OUTLINE MS-012AA.
5. Dimension does not include mold protrusions, which dot not exceed 0.15 [0.006].
6. Dimension does not include mold protrusions, which dot not exceed 0.25 [0.010].
7. Dimension is the length of lead for soldering to a certain substrate.